

**Amendments to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application:

**Listing of the Claims:**

1. (Currently Amended) An apparatus comprising:  
  
a buffer having at least one trigger, integrated on a component connected with a simultaneous bi-directional (SBD) memory bus having ternary logic levels, to observe and echo a predetermined finite set of bi-direction signals transmitted on said memory bus, ~~signals transmitted into said component and signals transmitted out of said component;~~  
  
~~wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus.~~
  
2. (Original) The apparatus as in claim 1, further comprising an observability port coupled with said buffer to receive said echoed signals, an observability bus connected with said observability port, and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

3. (Original) The apparatus as in claim 2, wherein said observability port is a logic observability port.

4. (Canceled)

5. (Original) The apparatus as in claim 1, wherein said buffer configured to observe and echo signals transmitted by wireless communication.

6. (Currently Amended) A method comprising:

transmitting signals on a simultaneous bi-directional (SBD) memory bus  
having ternary logic levels;

a buffer having at least one trigger, integrated on a component connected with a the bus, observing and echoing a predetermined finite set of signals transmitted on the bus, ~~signals transmitted into the component and signals transmitted out of the component;~~

~~wherein said bus is one of a memory bus, a data bus, an address bus, and a control bus.~~

7. (Original) The method as in claim 6, further comprising:

receiving said echoed signals; and

performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

8. (Canceled)
9. (Original) The method as in claim 6, wherein said signals are transmitted by wireless communication.
10. (Currently Amended) A system comprising:
- a memory;
  - an input/output (I/O) port; and
  - a microprocessor;
- ~~wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus; and~~
- a buffer means, integrated on a component coupled to one of said busses, for observing and echoing a predetermined finite set of signals transmitted on a bus simultaneous bi-directional (SBD) memory bus having ternary logic levels, ~~signals transmitted into the component and signals transmitted out of said component.~~
11. (Original) The system as in claim 10, further comprising means for receiving said echoed signals, and means for performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

12. (Canceled)

13. (Original) The system as in claim 10, wherein said signals are transmitted by wireless communication.

14. (Currently Amended) A system comprising:

a memory;

an input/output (I/O) port; and

a microprocessor;

~~wherein said memory, said I/O port, and said microprocessor are connected by a data bus, an address bus and a control bus; and~~

a buffer, having at least one trigger, integrated on a component coupled with a simultaneous bi-directional (SBD) memory bus having ternary logic level~~one of said busses~~, to observe and echo a predetermined finite set of bi-direction~~signals transmitted on said bus, signals transmitted into said component and signals transmitted out of said component.~~

15. (Original) The system as in claim 14, further comprising an observability port coupled with said buffer to receive said echoed signals, an observability bus connected with said observability port, and a diagnostic device being at least one of a logic analyzer and a bus analyzer connected with said observability bus and

performing at least one of detecting said echoed signals, accessing said echoed signals and reading said echoed signals.

16. (Original) The system as in claim 15, wherein said observability port is a logic observability port.

17. (Canceled)

18. (Currently Amended) The system as in claim 14, wherein said buffer is ~~configured~~ to observe and echo signals transmitted by wireless communication.